REMARKS

The Office Action dated May 23, 2005, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 3-4 have been amended, and claims 1-2 have been cancelled without prejudice. New claim 12 has been added. Applicants submit that the new claim as well as the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 3-5 and 12 are pending in the present application and are respectfully submitted for consideration. Claims 6-11 have been withdrawn from consideration.

Claims 1-5 Rejected under 35 U.S.C. § 102(b)

Claims 1-5 were rejected under 35 U.S.C. § 102(b) as being anticipated by Choi et al. (U.S. Patent No. 5,297,085, hereinafter "Choi"). Claims 1 and 2 have been canceled, and therefore the rejection with respect to these claims is now moot. As for the rejection of remaining claims 3-5, the rejection is respectfully traversed.

In one embodiment of the present invention, the regular memory cell array comprises plural redundant replacement units MCA0-3 for which the plural input/output circuit IO-0-3 are provided. And pre-charge switches are provided for the plural redundant replacement units and the redundant memory cell array RMCA. Further, the redundant replacement unit having a failed portion is replaced with the redundant memory cell array. And in case where a failed portion does not exist in the regular memory cell array, the pre-charge switches of the redundant replacement units are

enabled, and the pre-charge switch of the redundant memory cell array is not enabled, and in case where a failed portion exists in the regular memory cell array, the pre-charge switch of the redundant replacement unit having a failed portion is disabled and the pre-charge switches of the remaining redundant replacement units and the redundant memory cell array are enabled.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

Applicants submit that Choi merely provides only one of the regular memory blocks NBL1-NBL16 and the redundant memory block RBL becomes active, and only the corresponding precharge circuit NPC, RPC becomes active whereas the remaining precharge circuits become inactive.

Furthermore, in case no failed bit occurs in Choi, then no fuse is disconnected so that all signals FCRD1-16 are at L level. In case any one failed bit exists, then the corresponding fuse is disconnected, so that any of the signals FCRD1-16 becomes at L level. As shown in the redundant clock generator 22 of Choi (Fig. 11), when all memory cells are good, all FCRD1-16 are H level and the signal 163 is L level then Φ clbs is H level, and the regular memory block is selected and only precharge circuit of the selected memory block is enabled. When Φ rdbst is L level, the redundant memory block is not selected and the precharge circuit thereof is disabled.

On the other hand, when some memory cells fail of Choi, any one of RCRD1-16 is at L level and the signal 163 is at H level, then Φ rdbst is at H level, and the redundant memory block is selected and the precharge circuit is enabled, whereas Φ

clbs is L level, only the precharge circuit of the regular memory block which is selected by the block decoder 18 according to the signal LBS1-16 is enabled, and the precharge circuit of the unselected regular memory block is disabled.

Therefore, the SRAM in Choi has only a one-bit input/output structure. Accordingly, only one block among the 16 regular memory blocks and one redundant memory block is selected, and only the precharge circuit of the selected memory block is enabled. At the same time, only the sense amplifier and the column decoder of the selected memory block are enabled. Therefore, in Choi, only selected memory block and corresponding peripheral circuits are active so as to reduce the power consumption.

In contrast, the present invention has a plural input/output structure. Therefore, 16 memory units are active, for example. When there is a failed bit, the unit of the failed bit is replaced with the redundant memory cell array, and the unit of the failed bit and its precharge circuit becomes inactive, whereby the remaining units are all still active and the redundant memory cell array and its precharge circuit becomes active.

Applicants submit that the cited prior art fails to disclose each and every feature recited in claim 12 of the present application, and therefore is allowable.

As claims 3-5 depend from claim 12, Applicants submit that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claim, as well as for the additional subject matter recited therein.

Conclusion

In view of the above, Applicants respectfully submit that each of claims 3-5 and 12 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 3-5 and 12 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, referring to client-matter number 108066-00096.

Respectfully submitted,

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